

PS21997-4/-4A/-4C/-4W

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21997-4



INTEGRATED POWER FUNCTIONS

600V/30A low-loss CSTBT inverter bridge for three phase DC-to-AC power conversion

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

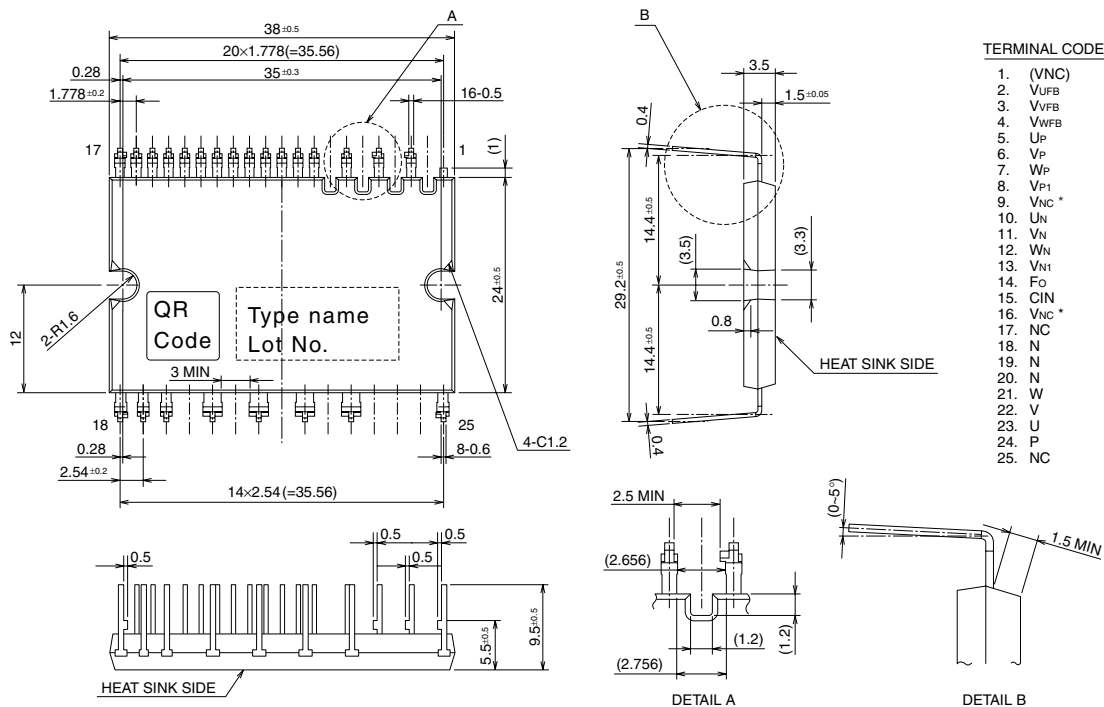
- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection.
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to a SC fault (N-side IGBT), a UV fault (N-side supply).
- Input interface : 3~5V line (High Active).
- UL Recognized : Yellow Card No. E80276

APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES (PS21997-4)

Dimensions in mm

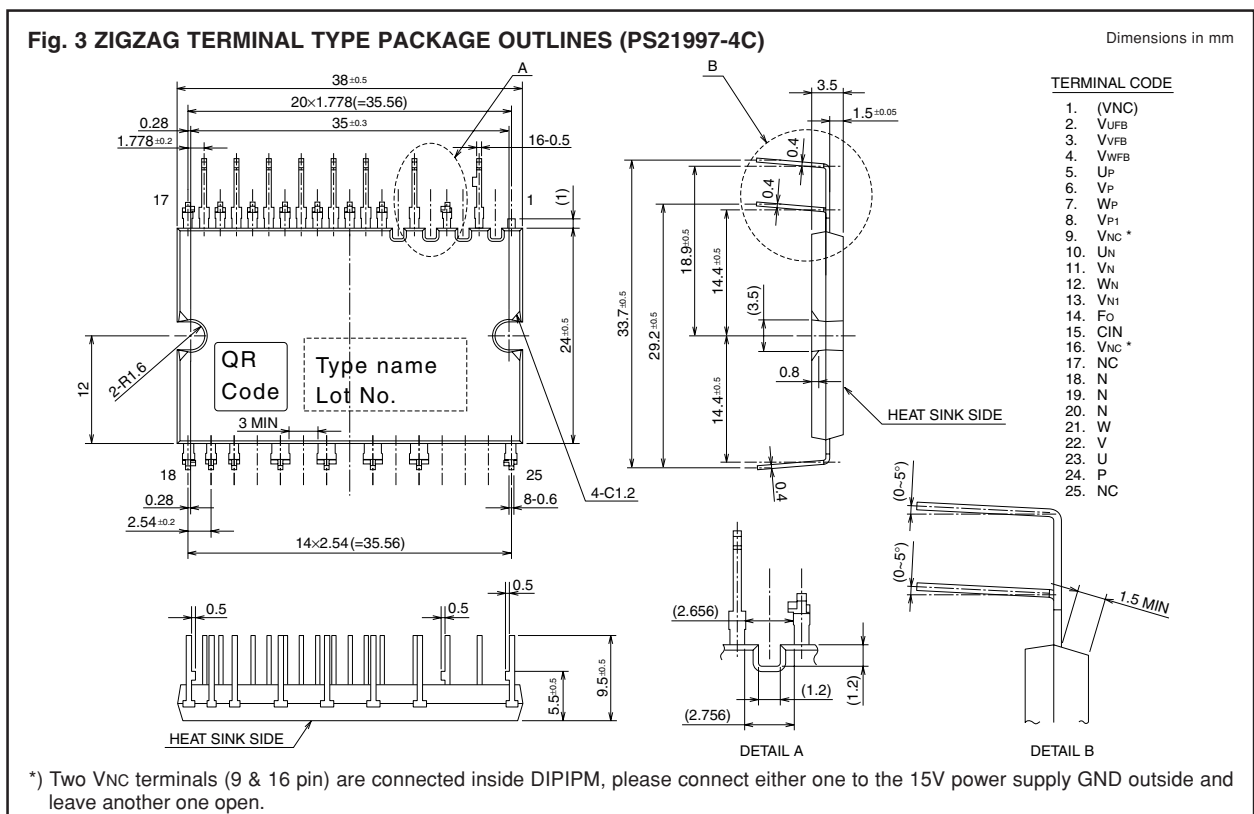
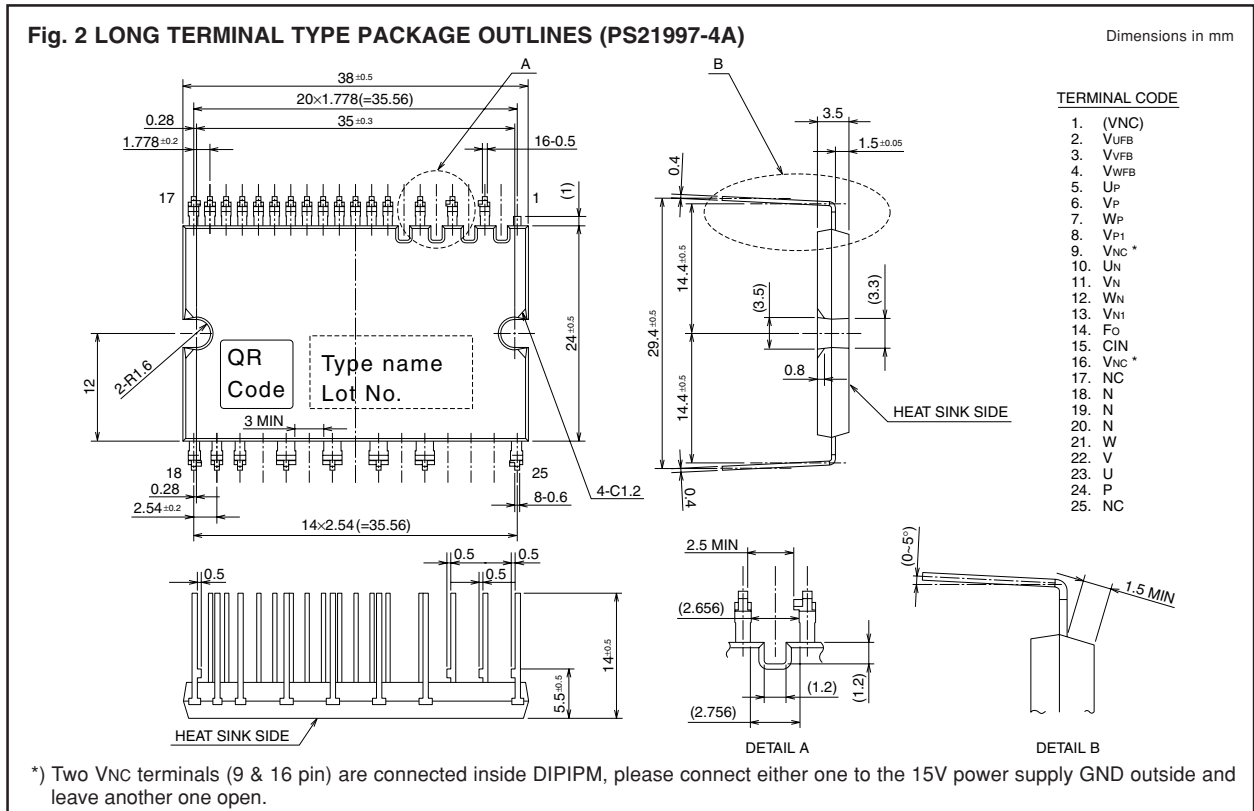


*) Two Vnc terminals (9 & 16 pin) are connected inside DIPIM, please connect either one to the 15V power supply GND outside and leave another one open.

Note : CSTBT is registered trademark of MITSUBISHI ELECTRIC CORPORATION in Japan.

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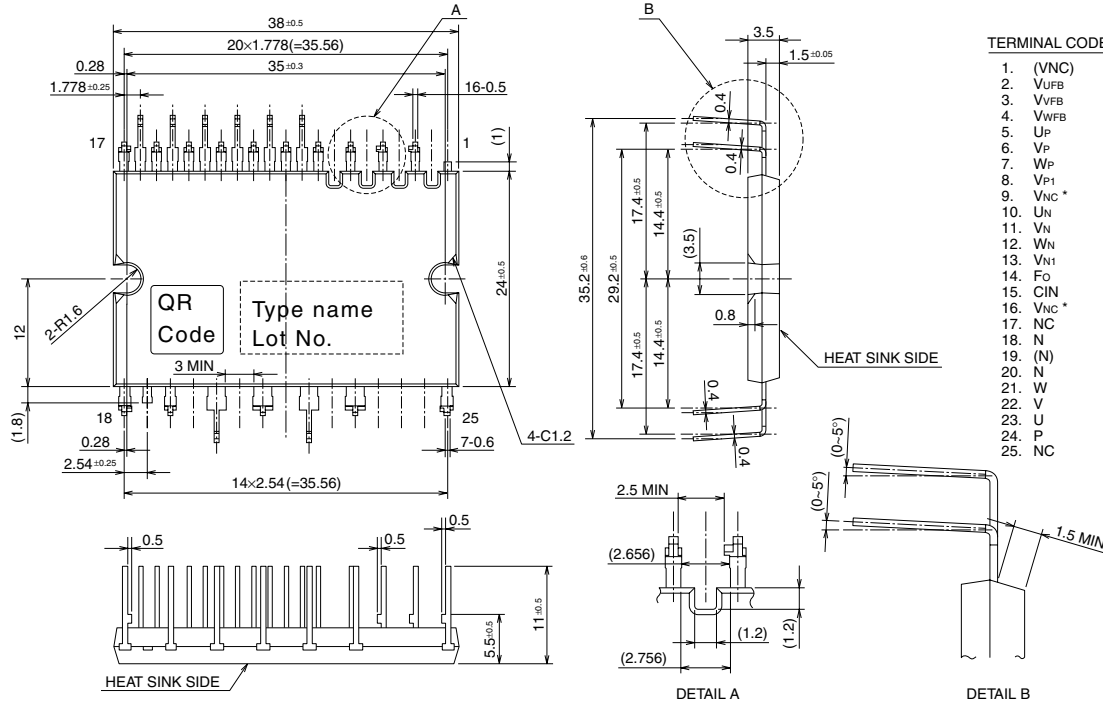


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Fig. 4 BOTH SIDES ZIGZAG TERMINAL TYPE PACKAGE OUTLINES (PS21997-4W)

Dimensions in mm

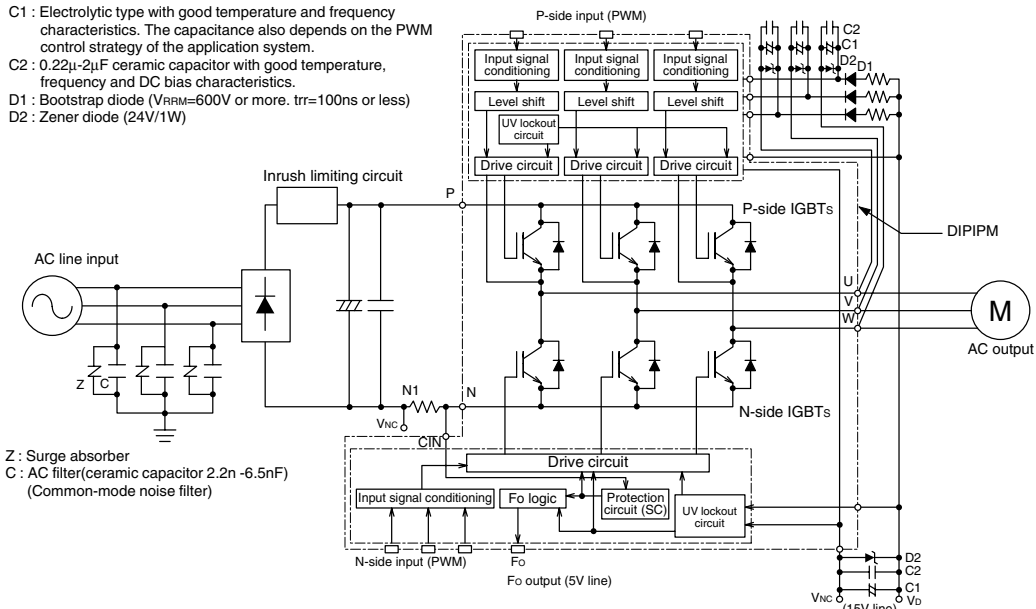


*) Two VNC terminals (9 & 16 pin) are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.

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Fig. 5 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

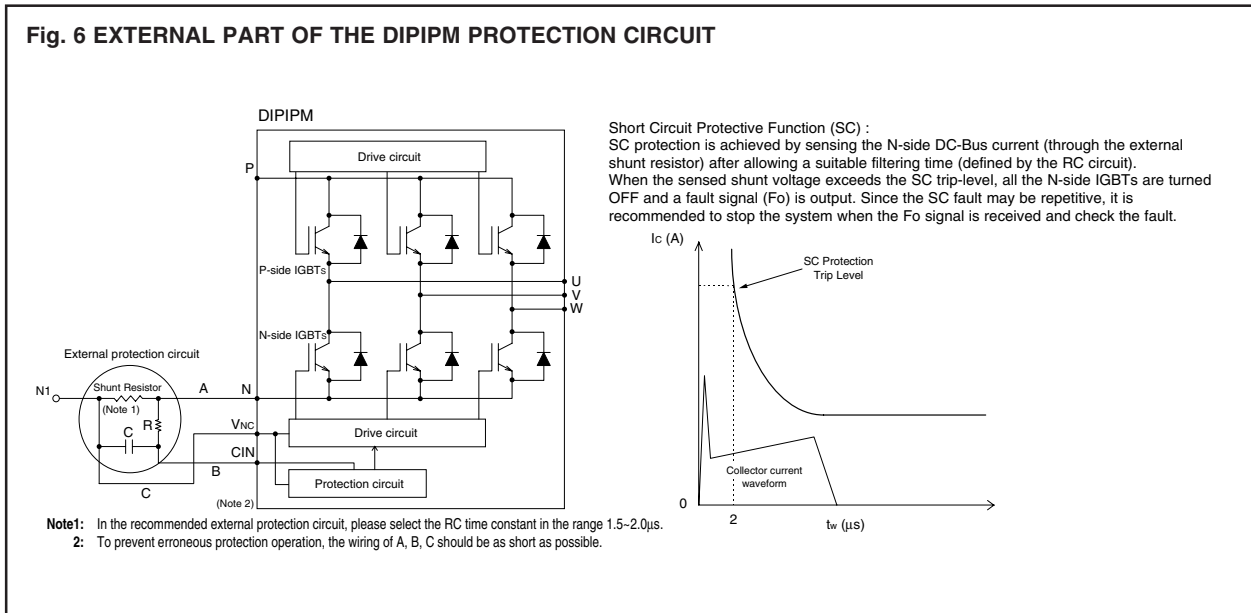
- C1 : Electrolytic type with good temperature and frequency characteristics. The capacitance also depends on the PWM control strategy of the application system.
- C2 : 0.22μ-2μF ceramic capacitor with good temperature, frequency and DC bias characteristics.
- D1 : Bootstrap diode (VRRM=600V or more, trr=100ns or less)
- D2 : Zener diode (24V/1W)



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Fig. 6 EXTERNAL PART OF THE DIIPM PROTECTION CIRCUIT



MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
VCC	Supply voltage	Applied between P-N	450	V
VCC(surge)	Supply voltage (surge)	Applied between P-N	500	V
VCEs	Collector-emitter voltage		600	V
±Ic	Each IGBT collector current	Tc = 25°C	30	A
±ICP	Each IGBT collector current (peak)	Tc = 25°C, less than 1ms	60	A
Pc	Collector dissipation	Tc = 25°C, per 1 chip	47.6	W
Tj	Junction temperature	(Note 1)	-20~+125	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIIPM is 150°C (@ Tc ≤ 100°C). However, to ensure safe operation of the DIIPM, the average junction temperature should be limited to Tj(ave) ≤ 125°C (@ Tc ≤ 100°C).

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
Vd	Control supply voltage	Applied between VP1-VNC, VN1-VNC	20	V
VDB	Control supply voltage	Applied between VUFB-U, VVFB-V, VWFB-W	20	V
VIN	Input voltage	Applied between UP, VP, WP, UN, VN, WN-VNC	-0.5~Vd+0.5	V
VFO	Fault output supply voltage	Applied between Fo-VNC	-0.5~Vd+0.5	V
Ifo	Fault output current	Sink current at Fo terminal	1	mA
Vsc	Current sensing input voltage	Applied between CIN-VNC	-0.5~Vd+0.5	V

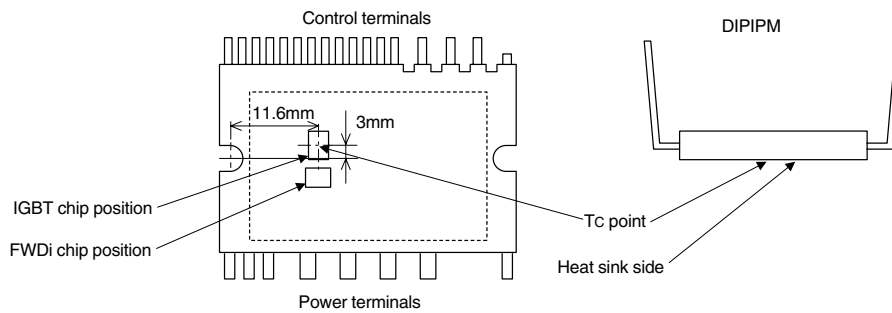
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TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(PROT)}	Self protection supply voltage limit (short circuit protection capability)	V _D = 13.5~16.5V, Inverter part T _j = 125°C, non-repetitive, less than 2μs	400	V
T _C	Module case operation temperature	(Note 2)	-20~+100	°C
T _{stg}	Storage temperature		-40~+125	°C
V _{iso}	Isolation voltage	60Hz, Sinusoidal, 1 minute, Between pins and heat sink plate	1500	V _{rms}

Note 2: T_C measurement point



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	2.1	°C/W
R _{th(j-c)F}		Inverter FWDi part (per 1/6 module)	—	—	3.0	°C/W

Note 3: Grease with good thermal conductivity and long-term quality should be applied evenly with +100μm~+200μm on the contacting surface of DIPIM and heat sink.

The contacting thermal resistance between case and heat sink (R_{th(c-f)}) is determined by the thickness and the thermal conductivity of the applied grease.

For reference, R_{th(c-f)} (per 1/6 module) is about 0.3°C/W when the grease thickness is 20μm and the thermal conductivity is 1.0W/mK.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CE(sat)}	Collector-emitter saturation voltage	V _D = V _{DB} = 15V V _{IN} = 5V	—	1.90	2.50	V
V _{EC}	FWDi forward voltage	T _j = 25°C, -I _C = 30A, V _{IN} = 0V	—	1.70	2.20	
t _{on}	Switching times	V _{CC} = 300V, V _D = V _{DB} = 15V I _C = 30A, T _j = 125°C, V _{IN} = 0 ↔ 5V Inductive load (upper-lower arm)	0.70	1.30	1.90	μs
t _{tr}			—	0.30	—	μs
t _{c(on)}			—	0.40	0.60	μs
t _{off}			—	1.70	2.65	μs
t _{c(off)}			—	0.40	1.00	μs
I _{CES}	Collector-emitter cut-off current	V _{CE} = V _{CES}	—	—	1	mA
		T _j = 125°C	—	—	10	

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CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I _D	Circuit current	V _D = V _{DB} = 15V V _{IN} = 5V	Total of V _{P1} -V _{NC} , V _{N1} -V _{NC}	—	—	2.80	mA
			V _{UFB-U} , V _{VFB-V} , V _{WFB-W}	—	—	0.55	mA
		V _D = V _{DB} = 15V V _{IN} = 0V	Total of V _{P1} -V _{NC} , V _{N1} -V _{NC}	—	—	2.80	mA
			V _{UFB-U} , V _{VFB-V} , V _{WFB-W}	—	—	0.55	mA
V _{FOH}	Fault output voltage	V _{SC} = 0V, F _O terminal pull-up to 5V by 10kΩ			4.9	—	V
V _{FOL}		V _{SC} = 1V, I _{FO} = 1mA			—	—	0.95
V _{SC(ref)}	Short circuit trip level	V _D = 15V (Note 4)	0.43	0.48	0.53	V	
I _{IN}	Input current	V _{IN} = 5V	0.70	1.00	1.50	mA	
UV _{DBt}	Control supply under-voltage protection	T _j ≤ 125°C	Trip level	10.0	—	12.0	V
UV _{DBr}			Reset level	10.5	—	12.5	V
UV _{Dt}			Trip level	10.3	—	12.5	V
UV _{Dr}			Reset level	10.8	—	13.0	V
t _{FO}	Fault output pulse width	(Note 5)	40	—	—	μs	
V _{th(on)}	ON threshold voltage	Applied between U _P , V _P , W _P , U _N , V _N , W _N -V _{NC}	—	2.1	2.6	V	
V _{th(off)}	OFF threshold voltage		0.8	1.3	—	V	
V _{th(hys)}	ON/OFF threshold hysteresis voltage		0.35	0.65	—	V	

Note 4: Short circuit protection works only for the N-side. Please select the external shunt resistance such that the SC trip-level is up to 1.7 times of the current rating.

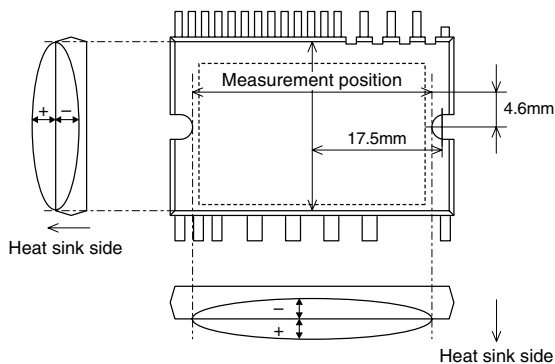
5: Fault signal is asserted only corresponding to a SC or a UV failure at N-side, and the F_O pulse width is different for each failure modes. For SC failure, F_O output is with a fixed width of 40μs(min), but for UV failure, F_O outputs continuously during the whole UV period, however, the minimum F_O pulse width is 40μs(min) for very short UV period less than 40μs.

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition	Limits			Unit
		Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 6) Recommended : 0.69 N·m	0.59	—	0.78	N·m
Weight		—	10	—	g
Heat-sink flatness	(Note 7)	-50	—	100	μm

Note 6: Plain washers (ISO 7089~7094) are recommended.

Note 7: Flatness measurement position



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RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
V _{CC}	Supply voltage	Applied between P-N	0	300	400	V	
V _D	Control supply voltage	Applied between V _{P1} -V _N C, V _{N1} -V _N C	13.5	15.0	16.5	V	
V _{DB}	Control supply voltage	Applied between V _U F _B -U, V _V F _B -V, V _W F _B -W	13.0	15.0	18.5	V	
ΔV _D , ΔV _{DB}	Control supply variation		-1	—	1	V/μs	
t _{dead}	Arm shoot-through blocking time	For each input signal, T _c ≤ 100°C	2.0	—	—	μs	
f _{PWM}	PWM input frequency	T _c ≤ 100°C, T _j ≤ 125°C	—	—	20	kHz	
I _o	Allowable rms current	V _{CC} = 300V, V _D = V _{DB} = 15V, P.F = 0.8, sinusoidal PWM, T _j ≤ 125°C, T _c ≤ 100°C (Note 8)	f _{PWM} = 5kHz	—	—	15.0	Arms
			f _{PWM} = 15kHz	—	—	11.0	
P _{WIN(on)}	Allowable minimum input pulse width	200V ≤ V _{CC} ≤ 350V, 13.5V ≤ V _D ≤ 16.5V, 13.0V ≤ V _{DB} ≤ 18.5V, -20°C ≤ T _c ≤ 100°C, N-line wiring inductance less than 10nH (Note 10)	(Note 9)	0.5	—	—	μs
P _{WIN(off)}			Below rated current	1.5	—	—	μs
			Between rated current and 1.7 times of rated current	3.0	—	—	
V _N C	V _N C variation	Between V _N C-N (including surge)	-5.0	—	5.0	V	

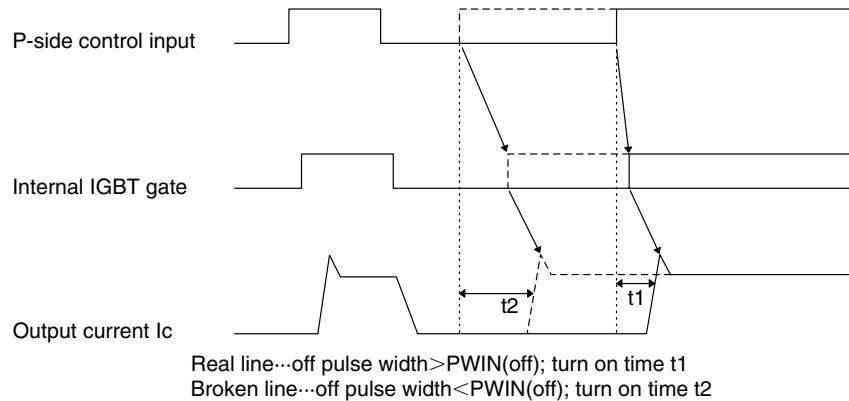
Note 8 : The allowable rms current value depends on the actual application conditions.

9 : Input signal with on pulse width less than P_{WIN(on)} might make no response.

10: Input signal with off pulse width less than P_{WIN(off)} might make no response, or make delayed response to P-side input only. (The delay is less than about 4μs.)

Please refer Fig.7 about delayed response and Fig.11 about N-line inductance.

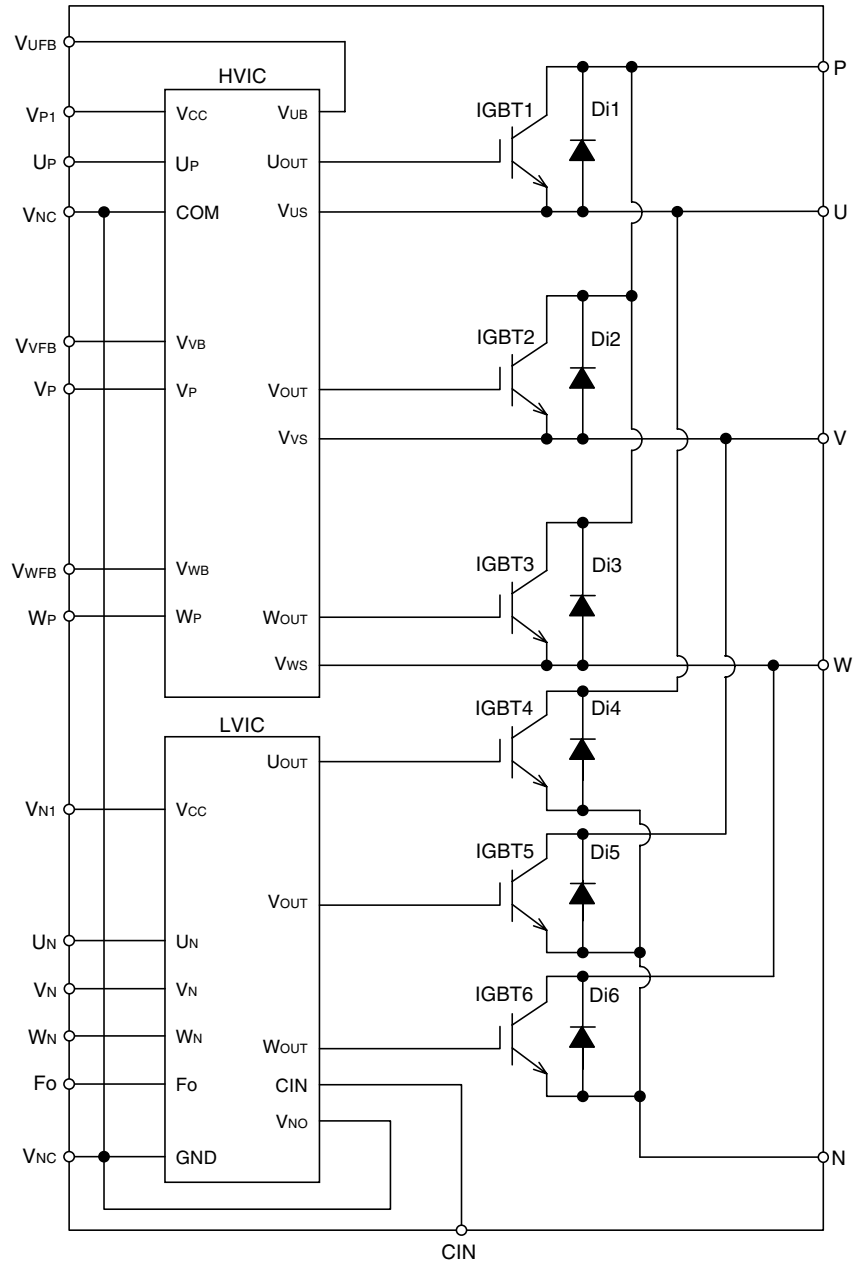
Fig. 7 About Delayed Response Against Shorter Input Off Signal Than P_{WIN(off)} (P-side only)



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Fig. 8 THE DIIPM INTERNAL CIRCUIT



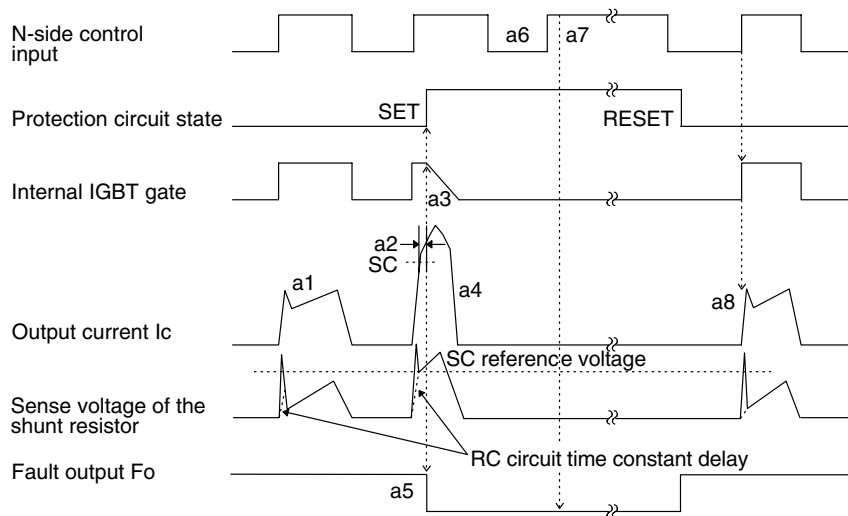
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Fig. 9 TIMING CHART OF THE PROTECTIVE FUNCTIONS

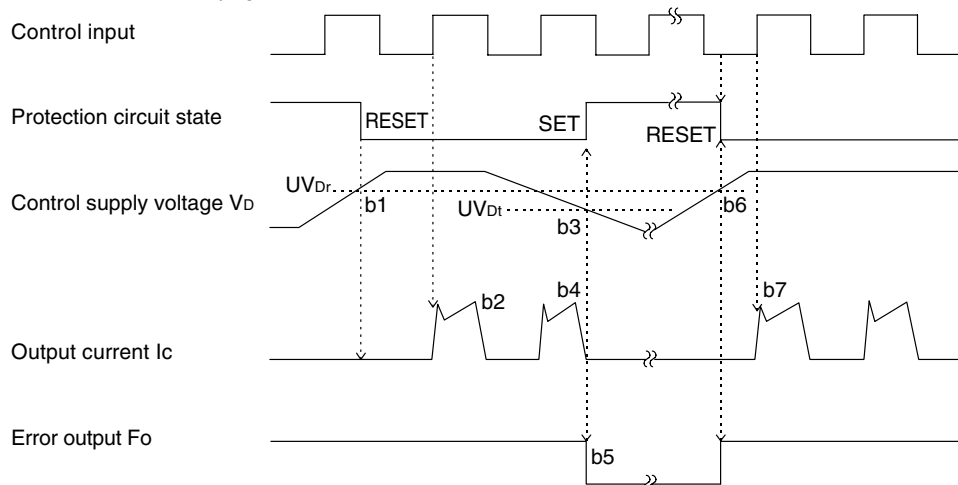
[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit is detected (SC trigger).
- a3. All N-side IGBTs' gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. Fo is output ($t_{FO(min)} = 40\mu s$).
- a6. Input "L".
- a7. Input "H". But IGBT is still OFF state during outputting Fo.
- a8. IGBT turns ON when L→H signal is input after Fo is reset.



[B] Under-Voltage Protection (N-side, UVd)

- b1. Control supply voltage V_D rises : After V_D level rises over under voltage reset level (UV_{Dr}), the circuits start to operate when next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. V_D level dips to under voltage trip level. (UV_{Dt}).
- b4. All N-side IGBTs turn OFF in spite of control input condition.
- b5. Fo is output. ($t_{FO} \geq 40\mu s$ and Fo outputs continuously during UV period).
- b6. V_D level rises over UV_{Dr} .
- b7. Normal operation : IGBT ON and carrying current.



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[C] Under-Voltage Protection (P-side, UVDB)

- c1. Control supply voltage VDB rises : After VDB level rises over under voltage reset level (UVDBr), the circuits start to operate when next input is applied.
- c2. Normal operation : IGBT ON and carrying current.
- c3. VDB level dips to under voltage trip level. (UVDBt).
- c4. P-side IGBT turns OFF in spite of control input signal level, but there is no Fo signal output.
- c5. VDB level rises over UVDBr.
- c6. Normal operation : IGBT ON and carrying current.

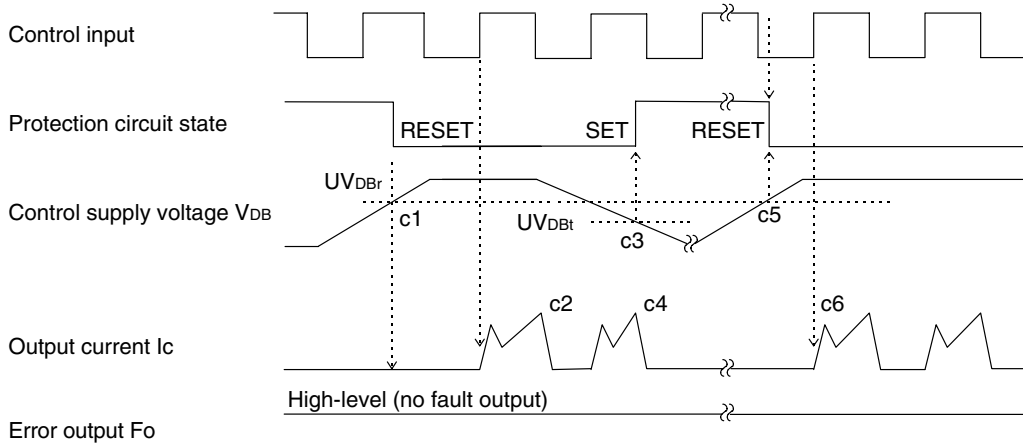
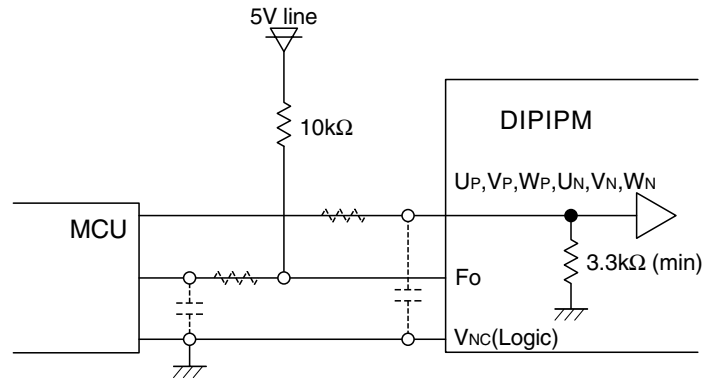
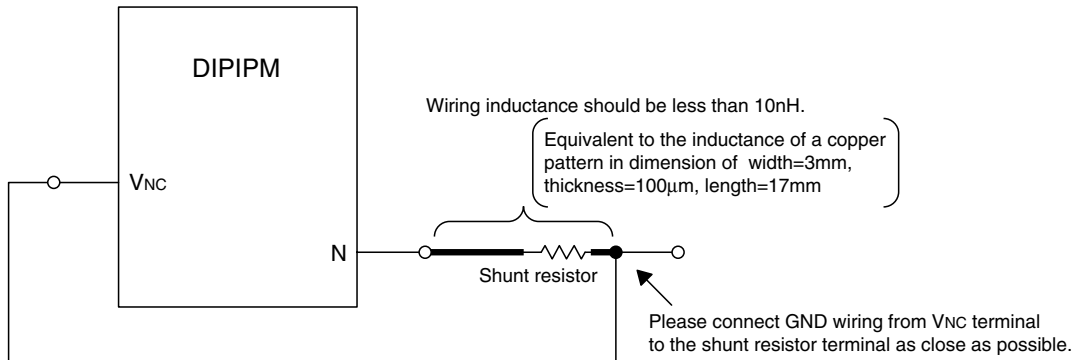


Fig. 10 AN INSTANCE OF INTERFACE CIRCUIT



Note : The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.
Input circuit integrates a 3.3kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

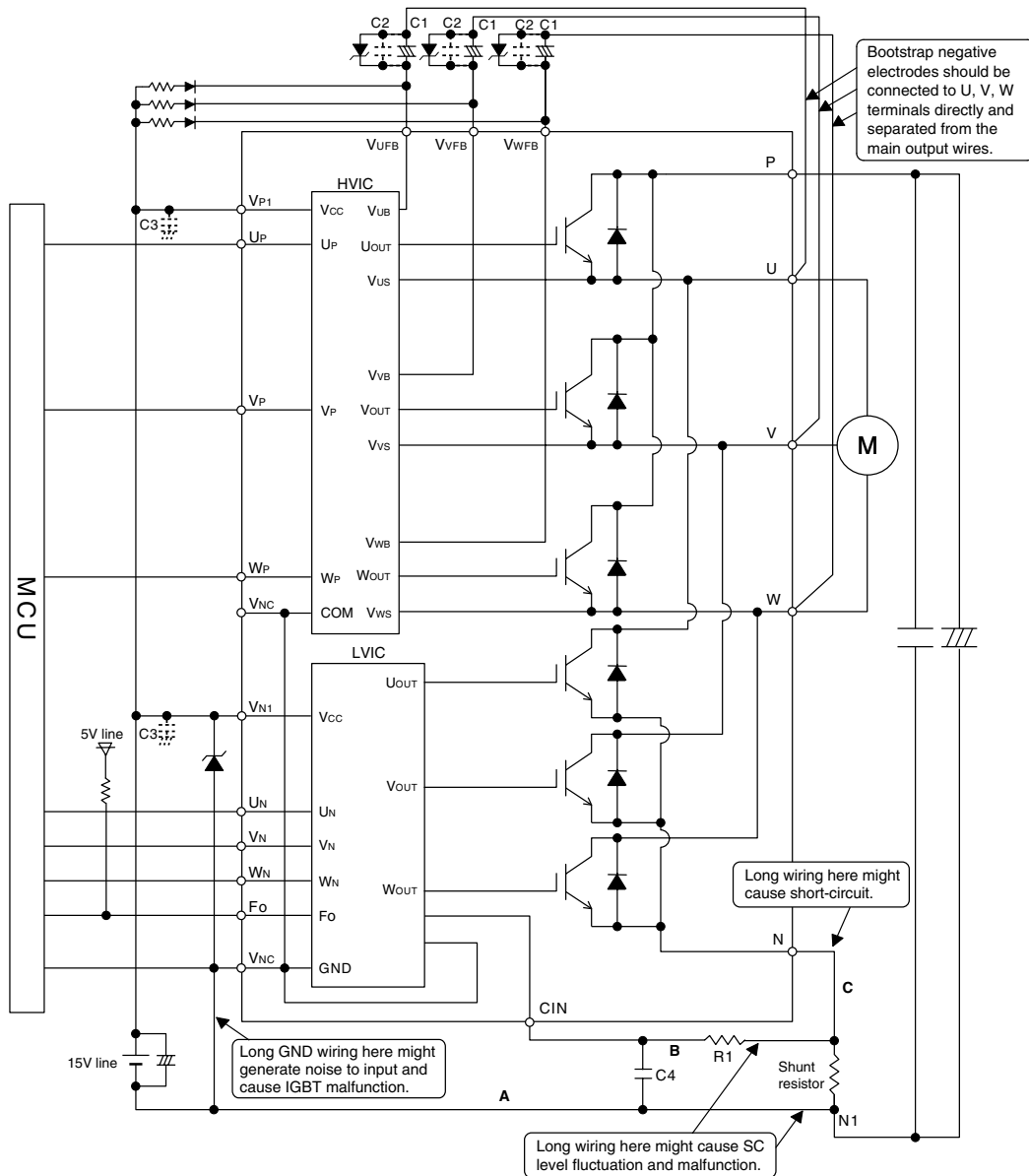
Fig. 11 WIRING CONNECTION OF SHUNT RESISTOR



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Fig. 12 AN EXAMPLE OF TYPICAL DIIPM APPLICATION CIRCUIT



- Note 1** : Input drive is High-active type. There is a 3.3kΩ (Min.) pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
- 2** : Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
- 3** : Fo output is open drain type. It should be pulled up to the MCU or control power supply (e.g. 5V, 15V) by a resistor that makes Ifo up to 1mA.
- 4** : To prevent erroneous protection, the wiring of A, B, C should be as short as possible.
- 5** : The time constant R1C4 of the protection circuit should be selected in the range of 1.5-2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1, C4
- 6** : All capacitors should be mounted as close to the terminals of DIIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2, C3 (0.22~2μF) : good temperature, frequency and DC bias characteristic ceramic type are recommended.)
- 7** : To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber between the P-N1 terminals is recommended.
- 8** : Two Vnc terminals (9 & 16 pin) are connected inside DIIPM, please connect either one to the 15V power supply GND and leave the other open.
- 9** : It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
- 10** : If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1.
- 11** : High voltage (VRRM =600V or more) and fast recovery type (trr=100ns or less) diodes should be used in the bootstrap circuit.